Session 29 Overview

Analog and Power Management Techniques





Chair: Doug Smith, *SMSC, Austin,TX*

Associate Chair: JoAnn Close, *Analog Devices, San Jose, CA*

Power management appears as a central theme among the nine papers in this session, which reflect a wide range of applications. Advances in the two amplifier designs reflect a combination of linear and switching techniques. Power efficiency and minimizing the use, size and cost of external components continue to be of paramount importance in switching converters.

Switching DC-DC converters, a staple of electronic systems for decades, were first constructed with discrete transistors and recently as standalone ICs. Now we see that that these key high-efficiency circuits are being embedded in larger SoCs to manage the multiple supply voltages and accuracy requirements of modern ICs. One of the main impediments to integrating these converters has always been the inductor required. Inductors are often bulky and expensive, and one external inductor is typically required for each output voltage. This challenge is being met with both an increase in switching speed while maintaining acceptable efficiency, and the generation of multiple outputs using just a single inductor.

Polar modulation schemes have significant potential for power savings in wireless transmitters, but place very stringent demands on the supply regulation systems. Paper 29.1 from KAIST and MagnaChip Semiconductor shows that the combination of linear and switching techniques that once was reserved for amplifiers in the audio range can be applied to deliver the control bandwidth required for EDGE modulation while keeping the efficiency high. In this design, the performance of the output stage of the linear amplifier, which modulates the PA supply, remains important as it must correct for the ripple of the switching amplifier.

Paper 29.2 from Georgia Tech and Paper 29.3 from U Brescia present advances in LDO and charge pump designs that highlight the fact that the control of power continues to be an important and active area in analog IC design.

Paper 29.4 from KU Leuven continues the theme in that a combination of linear and switching techniques is used to produce an ADSL central office line driver with low power dissipation. This paper advance previous work by increasing the sophistication of the feedback loop around the switching stage while maintaining the previously reported high supply voltage using low-voltage CMOS devices.

Paper 29.5 from U Pavia and austriamicrosystems, and Paper 29.9 from KAIST, KEC, and JDA Technology demonstrate various advances in control schemes in addition to the use of a single inductor. Paper 29.6 from Stanford and National Semiconductor describes a buck converter optimized to improve efficiency for light loads. The authors of Paper 29.7 from U Pisa describe a converter whose output changes in such a way that it makes the performance of the sub-threshold MOS circuits it drives less sensitive to process variations and temperature.

Paper 29.8 from U British Columbia realizes an embedded 3GHz DC-DC converter with fully integrated inductor, delivering higher overall system efficiency by combining the converter and the system clock tree, and recycling clock charge and delivering it to the load instead of ground.

 1-4244-0852-0/07/$25.00 ©2007 IEEE.



29.1 A 2W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters **1:30 PM**

T-W. Kwak, KAIST, Daejeon, Korea

An amplitude modulator for Class-E2 EDGE polar transmitters is fabricated in a 0.35μm CMOS process. This hybrid switching modulator consists of a Class-D amplifier with a 2MHz switching frequency and a wideband buffered analog amplifier having a low output impedance of 200mΩ at high frequency. It can drive an RF PA with an equivalent impedance of 4Ω up to maximum output power of 2.25W with a maximum efficiency of 88.3%. The chip area is 4.7mm^2.



29.2 A 5mA 0.6μm CMOS Miller-Compensated LDO Regulator with -27dB Worst-Case Power-Supply Rejection Using 60pF of On-Chip Capacitance **2:00 PM**

V. Gupta, Georgia Institute of Technology, Atlanta, GA

A 0.6μm 1.8V 5mA Miller-compensated SoC LDO regulator uses 60pF of capacitance to achieve a worst-case power-supply rejection of -27dB over 50MHz. The entire regulator is shielded from fluctuations in the supply using an NMOS cascode that is biased using a charge pump, voltage reference, and RC filter to maintain low dropout. The RC filter establishes a stable bias for the cascode without a significant impact on the efficiency or bandwidth of the LDO regulator.



29.3 A 1.2-to-8V Charge-Pump with Improved Power Efficiency for Non-Volatile Memories **2:15 PM**

A. Richelli, University of Brescia, Brescia, Italy

A charge-pump architecture is presented with an improved power efficiency and a high voltage output compared to the known Dickson and Favrat architectures due to partial reuse of the charge stored on the capacitors. An 8-stage charge pump fabricated in a 0.13μm CMOS process has a 1.2V supply and a 100MHz clock. The measured performance indicates that the efficiency can be 25% higher than a Favrat cell. The efficiency increases with the number of stages, reaching 60% with 10 stages.



29.4 A 237mW ADSL2+ CO Line Driver in a Standard 1.2V 0.13μm CMOS **2:30 PM**

B. Serneels, KU Leuven, Leuven, Belgium

An ADSL2+ CO line driver with a 5.5V output buffer is implemented in a standard 1.2V 0.13μm CMOS technology. The line driver has an MTPR of 58dB and an efficiency of 42% for driving ADSL2+ signals with an average output power of 20dBm and a crest factor of 5.6. The 5.5V output buffer is designed with only digital active CMOS elements without the use of extra masks.



29.5 A 200mA 93% Peak Efficiency Single-Inductor Dual-Output DC-DC Buck Converter **3:15 PM**

E. Bonizzoni, University of Pavia, Pavia, Italy

A single-inductor dual-output DC-DC buck converter is presented. The inductor, which is external, provides two independent output voltages ranging from 1.2V to the power supply with a maximum total output current of 200mA. The supply can range from 2.6 to 5V. The converter is fabricated in a 0.35μm p-substrate CMOS technology. Measurement results demonstrate that a peak power efficiency as high as 93.3% can be achieved and the efficiency is always >62.5%.



29.6 A 3MHz Low-Voltage Buck Converter with Improved Light Load Efficiency **3:45 PM**

M. Mulligan, Stanford University, Stanford, CA, and National Semiconductor, Santa Clara, CA

A low-voltage synchronous buck converter has been designed and fabricated in a 0.5μm CMOS technology. The converter uses two charge conservation techniques to increase efficiency at light loads while still operating in PWM mode at a switching frequency of 3MHz. These techniques reduce IC power loss from 11.5mW to 8.9mW, a 22.7% reduction, for I_{load} = 20mA and V_{out} = 1.8V.



29.7 A Voltage Regulator for Subthreshold Logic with Low Sensitivity to Temperature and Process Variations **4:15 PM**

G. De Vita, Università di Pisa, Pisa, Italy

The V_0 of a voltage regulator changes with temperature and process variations to make the performance of subthreshold MOS logic almost insensitive to them. The propagation delay of a subthreshold CMOS inverter supplied by this regulator has a temperature sensitivity of 114ppm/°C and a relative standard deviation due to process variations of 4.9%. The regulator is fabricated in a 0.35μm process and draws 2.9 to 3.4μA from 1.8 to 4.3V over the 0 to 80°C range.



29.8 A 3GHz Switching DC-DC Converter Using Clock-Tree Charge-Recycling in 90nm CMOS with Integrated Output Filter **4:30 PM**

M. Alimadadi, University of British Columbia, Vancouver, Canada

A 90nm buck converter is intended for complex multi-core ICs. Using the 3GHz system clock for switching reduces the area to 0.27mm^2 and allows the output filter to be integrated. Efficiency is increased by recycling clock charge and delivering it to the load instead of ground. A dedicated 3GHz clock circuit driving 12pF consumes 39.9mW. In contrast, a combined clock and converter circuit consumes 56.2mW and delivers 25.7mW at the converter output. Regulation is achieved through PWM of the clock. The circuit converts 1.0V to between 0.5 to 0.7V at 40 to 100mA.



29.9 A Single-Inductor Switching DC-DC Converter with 5 Outputs and Ordered Power-Distributive Control **4:45 PM**

H-P. Le, KAIST, Daejeon, Korea

An integrated 5-output single-inductor multiple-output DC-DC converter with ordered power-distributive control in a 0.5μm BiCMOS process is presented. The converter has four main positive boost outputs programmable from +5 to +12V and one dependent negative output from -12 to -5V. A maximum efficiency of 80.8% is achieved at a total output power of 450mW, with a switching frequency of 700kHz.